Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (original) A method for processing data using a programmable processor comprising:

decoding a single instruction for writing data to memory specifying both a mask and a register containing data, the mask comprising fields that each correspond to a field of the data contained in the register;

detecting some of the fields of the mask as having a predetermined value and identifying corresponding fields of the data contained in the register as write-enabled data fields; and

writing the write-enabled data fields to a specified memory location.

2. (original) The method of claim 1 wherein each of the fields of the mask has a width of one bit.

3. (original) The method of claim 1 wherein each of the fields of the data contained in the register has a width of one bit.

4. (original) The method of claim 1 wherein the writing step further comprises reading an unaltered field of data from the specified memory location and writing the unaltered field of data along with the write-enabled data fields to the specified memory location.

5. (original) The method of claim 1 wherein the mask is contained in a specified register.

6. (original) The method of claim 1 wherein the memory location is contained in a specified register.

7. (original) The method of claim 1 wherein the specified memory location comprises a section of memory having a specific width and beginning at a specific memory address.

8. (original) The method of claim 1 wherein the predetermined value is a logic 1.

9. (original) The method of claim 1 further comprising:

decoding a second single instruction specifying a third and a fourth register each containing a plurality of floating-point operands;

multiplying the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality or products;

and providing the plurality of products to partitioned fields of a result register as a catenated result.

10. (currently amended) A computer-readable storage medium having stored therein a plurality of instructions that cause a computer processor to perform data operations:

~~having instructions that instruct a computer system to perform operations,~~

at least some of the instructions including a store multiplex instruction for selectively storing data in a programmable processor, the store multiplex instruction capable of instructing a computer to perform operations comprising:

decoding the store multiplex instruction specifying both a mask and a register containing data, the mask comprising fields that each correspond to a field of the data contained in the register;

detecting some of the fields of the mask as having a predetermined value and identifying corresponding fields of the data contained in the register as write-enabled data fields; and

writing the write-enabled data fields to a specified memory location.

11. (currently amended) The computer-readable storage medium of claim 10 wherein each of the fields of the mask has a width of one bit.

12. (currently amended) The computer-readable storage medium of claim 10 wherein each of the fields of the data contained in the register has a width of one bit.

13. (currently amended) The computer-readable storage medium of claim 10 wherein the writing step further comprises reading an unaltered field of data from the specified memory

location and writing the unaltered field of data along with the write-enabled data fields to the specified memory location.

14. (currently amended) The computer-readable storage medium of claim 10 wherein the mask is contained in a specified register.

15. (currently amended) The computer-readable storage medium of claim 10 wherein the memory location is contained in a specified register.

16. (currently amended) The computer-readable storage medium of claim 10 wherein the specified memory location comprises a section of memory having a specific width and beginning at a specific memory address.

17. (currently amended) The computer-readable storage medium of claim 10 wherein the predetermined value is a logic 1.

18. (currently amended) The computer-readable storage medium of claim 10 wherein at least some of the instructions further include a group floating point multiply instruction for multiplying floating point data in a programmable processor, the group floating point multiply instruction capable of instructing the computer to perform operations comprising:

decoding the group floating point multiply instruction specifying a third and a fourth register each containing a plurality of floating-point operands;

multiplying the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality or products; and

providing the plurality of products to partitioned fields of a result register as a catenated result.

19-27. (canceled)

28. (new) A method for processing data in a programmable processor, the method comprising:

decoding a single instruction for performing a bitwise insert operation on data in registers in a register file within the programmable processor, the bitwise insert operation operating on a first operand and a second operand stored in registers in the register file; and

for each bit in the first operand, the bitwise insert operation inserting the bit into a corresponding bit position in a destination value if a corresponding bit in the second operand has a first predetermined value.

29. (new) The method of claim 28 wherein the first predetermined value is a logic 1.

30. (new) The method of claim 28 wherein for each bit in the first operand, a corresponding bit position in the destination value is maintained as unchanged if a corresponding bit in the second operand has a second predetermined value.

31. (new) The method of claim 30 wherein the second predetermined value is a logic 0.

32. (new) The method of claim 28 further comprising a step of storing the destination value into memory.

33. (new) The method of claim 28 wherein each of the first and second operands has a width of 64 bits.

34. (new) The method of claim 28 further comprising a step of executing a plurality of different group floating-point arithmetic operations that arithmetically operate on multiple floating-point operands stored in partitioned fields of an operand register in the plurality of registers to produce a catenated result that is returned to a register in the plurality of registers, wherein the catenated result comprises a plurality of individual floating-point results.

35. (new) A computer-readable storage medium having stored therein a plurality of instructions that cause a computer processor to perform operations on data stored in registers in the computer processor, the plurality of instructions comprising:

an instruction that causes the processor to perform a bitwise insert operation on data in registers in a register file within the programmable processor, the bitwise insert operation operating on a first operand and a second operand stored in registers in the register file; and

wherein for each bit in the first operand, the bitwise insert operation inserts the bit into a corresponding bit position in a destination value if a corresponding bit in the second operand has a first predetermined value.

36. (new) The computer-readable storage medium of claim 35 wherein the first predetermined value is a logic 1.

37. (new) The computer-readable storage medium of claim 35 wherein for each bit in the first operand, a corresponding bit position in the destination value is maintained as unchanged if a corresponding bit in the second operand has a second predetermined value.

38. (new) The computer-readable storage medium of claim 37 wherein the second predetermined value is a logic 0.

39. (new) The computer-readable storage medium of claim 35 wherein the destination value is stored into memory.

40. (new) The computer-readable storage medium of claim 35 wherein each of the first and second operands has a width of 64 bits.

41. (new) The computer-readable storage medium of claim 35 wherein the plurality of instructions further comprises a plurality of different group floating-point arithmetic operations that arithmetically operate on multiple floating-point operands stored in partitioned fields of an operand register in the plurality of registers to produce a catenated result that is returned to a register in the plurality of registers, wherein the catenated result comprises a plurality of individual floating-point results.